Low Thermal Resistance Flip-Chip Bonding of 850 nm 2-D VCSEL Arrays Capable of 10 Gbit/s/ch Operation

Hendrik Roscher∗

In 2003, our well established technology of flip-chip mounted 2-D 850 nm backside-emitting VCSEL arrays evolved to bring about substantial thermal improvements. We have reduced the oxide-confined VCSEL’s thermal resistance by half, to a value of about 1.3 K/mW for 10 µm devices. An optimized solder joint placement eliminates the major thermal bottlenecks within the flip-chip VCSEL structure. The thermal performance of the improved cell design is compared to the previous version for devices with 250 µm pitch in 4 × 8 and 8 × 8 arrays. Neighboring VCSELs within these arrays are also shown to be thermally isolated with thermal cross resistances of about 0.015 K/mW. Furthermore, quasi error-free (bit error rate < 10^{-12}) 10 Gbit/s transmission was demonstrated by feeding the signals to the flip-chip mounted VCSELs through 7 mm-long coplanar transmission lines on a silicon carrier chip.

1. Introduction

Vertical-cavity surface-emitting lasers (VCSELs) arranged in two-dimensional (2-D) configurations of independently addressable elements hold great potential for short-reach fiber-optic as well as free-space networking applications. Given the continuous growth of required data rates in networks, parallel optical interconnects (POIs) based on VCSEL arrays are expected to be found more and more at increasingly deeper network levels in the future.

First 2-D arrays were InGaAs quantum well based, emitting at wavelengths around 980 nm. While readily allowing backside emission through the GaAs substrate, low-cost Si based photodetectors have extremely poor sensitivities for wavelengths approaching 1 µm. Today’s short-reach optical interconnect applications therefore rely on the standardized 850 nm emission wavelength regime. As far as single devices or linear arrays are concerned, wire bonding is typically used for contacting and top side emission is perfectly acceptable. Yet, for 2-D solutions high-speed electrical signals often cannot be fed to the VCSELs from external contacts and flip-chip bonding is the solution of choice to provide low parasitics electrical interconnects. Bottom side emitting VCSELs particularly lend

themselves to the flip-chip integration of large 2-D arrays. They naturally direct the electrical and optical domains to opposite sides of the VCSEL chip. Hence, the optics do not get in the way of the electronics and the benefits of the flip-chip approach are therefore best utilized with bottom-emitting VCSELs. The GaAs substrate, however, is opaque at 850 nm and the need to completely remove or replace it does add additional complexity to the fabrication of 850 nm bottom-emitting VCSEL arrays.

The details of flip-chip assembly and substrate removal were given in last year’s report. In what follows, the focus is placed on design changes leading to thermal improvements along with the implications of these changes for crucial device characteristics such as spectral red shift and optical output power. Error-free 10 Gbit/s data transmission will also be demonstrated.

2. Low Thermal Resistance Device-Level Packaging

In the early stages of development of this flip-chip technology, a lateral offset was introduced between the VCSEL mesa and the bond pads in order to keep the solder joints away from the active structures. This offset-bonded design illustrated in the left half of Fig. 1 ensures that no stresses arising from coefficient of thermal expansion mismatches between the joined substrates would adversely affect the VCSEL performance. The lateral offsets necessitate three levels of metallization and separate polyimide layers functioning both as planarization and non-wettable layer. The additional complexity of this design enables a simple incorporation of a plating base required for electroplating metal layers which is a more cost efficient way of metal deposition than evaporation or sputtering. The offset-bonded design also ensures that the bond pads are at exactly the same elevation and on a perfectly even surface.

![Diagram of offset-bonded and direct-bonded VCSEL designs.](image-url)
The development of stable bond pads serving as foundation for the solder joints, the use of soft indium solder, and precise bump size control permitted direct mesa bonding as indicated in the right-hand schematic of Fig. 1. This design involves different bump sizes for the n- and p-solder joints and can thus accommodate uneven bond pads at different mean elevations (omitted in the figure).

The indium solder is deposited by evaporation and structured by lift-off since, in contrast to electroplating which is also available for indium, it offers a tight control of the deposited heights as well as the additional freedom to vary the bump sizes by utilizing more or less of the area between the bond pads. The footprints of the evaporated solder deposits can have many different shapes, such as in Fig. 2, and with a given difference in footprint area the standoff difference between the p- and n-solder joints is adjusted by the applied solder thickness. Indium lift-off was done for thicknesses ranging from 3 to 12 µm. The structured deposits in Fig. 2 have a thickness of only 4 µm and side lengths of about 100 µm. Despite of this relatively high aspect ratio, the indium reliably flows to form evenly shaped balls on subjecting it to high temperatures above its melting point of approximately 160 °C. The visible dents become more pronounced with shorter cool-down cycles after reflow. Fortunately, they do not seem to have a negative effect on the bonding yield.

![Fig. 2: Evaporated indium deposits after lift-off structuring.](image1)

![Fig. 3: Indium solder balls after reflow. The p-solder ball sits on top of the n-mesa, and the p-mesa is inside the solder ball.](image2)

Indium solder, being a pure metal, has high thermal and electrical conductivities. Furthermore, no alloy related problems like decomposition leading to brittle high resistivity connections can occur. Its particular softness allowed the p-part of the VCSEL mesa to actually be fully inside the solder ball which partially sits on top of the n-mesa as the left half of Fig. 3 shows. To completely enclose the low mobility p-side of the VCSELs, where most of the heat is generated, is a possibility that is only available to bottom-emitting VCSELs. By eliminating some major thermal bottlenecks, the direct-bonded design leads to a substantially improved thermal performance of the VCSELs which will be further discussed in the following section.
3. Static Characteristics

Figure 4 compares the thermal performance of the two flip-chip bondable VCSEL designs discussed so far. The lateral paths in the offset-bonded VCSELs hamper the heat transport within the structure and result in a rather high thermal resistance $R_T$ of 2.6 K/mW for the 10 µm diameter lasers which is the only size available for this design. We measured a sample of 15 VCSELs in each of three $8 \times 8$ arrays and found the value highly reproducible with about 0.05 K/mW standard deviation. The large $R_T$ leads to a drastic junction temperature ($T_j$) rise during operation, e.g. $\Delta T_j \approx 50$ K at 10 mA laser current, which causes a pronounced red-shift of the output spectra displayed in the upper part of Fig. 5. Higher internal temperatures generally shorten the lifetime of these devices.

![Fig. 4: Measured thermal resistances for various sizes of the direct-bonded VCSELs, and for 10 µm offset-bonded VCSELs.](image)

![Fig. 5: Comparison of the spectral red shifts of different wafers in offset-bonded (top) and direct-bonded (bottom) configuration.](image)

For the direct-bonded VCSELs, there were 8 different aperture sizes fabricated within $4 \times 8$ element arrays. The data in Fig. 4 demonstrate the thermal resistance was cut by half to about 1.3 K/mW for 10 to 10.5 µm devices merely through elimination of thermal bottlenecks in the signal path within the cell design. Of course the high-frequency performance is expected to also benefit from streamlining the signal path.

In a real world application, all channels of the arrays are intended to be operated in parallel. It is therefore essential, besides having low thermal resistances, to ensure minimal thermal crosstalk between immediate neighbors not only to prevent signal degradation, but chiefly to prevent thermal breakdown during operation. If a VCSEL would use additional paths through neighboring cells for heat extraction, the array with all cells operating would quickly overheat. Hence, it is important that the thermal resistances presented above account only for heat paths within one cell.
In the current design, the VCSELs are thermally connected only through a very thin semiconductor layer over a distance of 250 µm. The resulting thermal cross resistances $R_{TX}$ are 0.016 K/mW and 0.013 K/mW for the offset-bonded and direct-bonded VCSELs, respectively. For extremely closely spaced VCSELs that are supposed to be operated simultaneously, a good thermal isolation would have to be maintained by completely separating the VCSELs from one another.

Figure 5 compares the spectral red shifts of VCSEL arrays made from different epitaxial material. The magnitude of the spectral shift $\Delta \lambda$ is approximately 2.5 nm for both the offset-bonded and direct-bonded configurations. At the same operating point, the internal temperature rise is the same for both designs. The reason for this is that epitaxy B of the direct-bonded VCSELs was optimized for a high differential quantum efficiency $\eta_d$. As Fig. 7 reveals, the optical field benefited from the optimization resulting in an $\eta_d$ as high as 75%, but at the expense of inferior electrical properties. The electrical resistance was drastically increased to about 350 Ω leading to twice the dissipated power.

Nevertheless, a much higher maximum output power is obtained from those VCSELs as compared to the offset-bonded VCSELs in Fig. 6 due to their thermally optimized packaging. Enhanced heat extraction in the direct-bonded configuration makes it possible to turn the high $\eta_d$ into a high maximum wallplug efficiency $\eta_{c,max}$ of 28% at 3 mA and a maximum output power of 9 mW at 12 mA. Figure 6 displays the complete light–current–voltage (LIV) curves of an offset-bonded array where epitaxy A was used. The differential resistance of those devices has a more typical value of 40 Ω leading to much less dissipated power. But due to the doubled thermal resistance these devices heat up quickly as well and with a low differential quantum efficiency of 30% the maximum wallplug efficiency is reached with 20% at 5 mA and the output power levels off at 5 mW and 18 mA.
4. Dynamic Performance of Flip-Chip VCSEL Demonstrators

The modulation characteristics of the flip-chip bonded VCSELs have been measured with a microwave probe placed at the far ends of the about 7 mm-long coplanar transmission lines on the fanout chip as indicated by the inset of Fig. 8. The parasitics of the lines are superimposed on the VCSEL resonant curves and the transfer functions therefore have maximum small-signal 3-dB and 10-dB bandwidths of 7 GHz at 6 mA and 9.4 GHz at 10 mA of operating current, respectively. Note that the photoreceiver has a 3-dB bandwidth of 8 GHz.

Digital data transmission experiments were conducted using that same setup. The curves in Fig. 9 demonstrate that quasi error-free (bit error rate < $10^{-12}$) 10 Gbit/s transmission was achieved. Although the present eye opening does not entirely conform to the indicated mask according to the IEEE 802.3ae 10-Gigabit Ethernet standard, there is much room for improvement through optimization of the fanout design and VCSEL dynamics.

5. Conclusion

Low thermal resistance direct mesa flip-chip bonding of VCSEL arrays was explained. The elimination of thermal bottlenecks by this approach cuts the thermal resistance by half to about 1.3 K/mW for 10 µm devices as compared to the offset-bonded devices. Neighboring cells (250 µm pitch) within the arrays are thermally isolated with thermal crosstalk values of about 0.015 K/mW.

To judge the dynamic performance, microwave signals are fed to the high-speed VCSELs through about 7 mm long low-loss coplanar transmission lines incorporated in the VCSEL demonstrator. The parasitics of the lines are superimposed on the VCSEL resonant curves which results in transfer functions exhibiting 3-dB and 10-dB corner frequencies of 7.0 and 9.4 GHz, respectively. Quasi error-free (bit error rate < $10^{-12}$) 10 Gbit/s digital data transmission was achieved.